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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,255	01/17/2001	William L. Betts	061607-1361	8278
24504	7590	06/06/2005	EXAMINER	
THOMAS, KAYDEN, HORSTEMEYER & RISLEY, LLP 100 GALLERIA PARKWAY, NW STE 1750 ATLANTA, GA 30339-5948			LUGO, DAVID B	
			ART UNIT	PAPER NUMBER
			2637	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/766,255

Applicant(s) ☒

BETTS, WILLIAM L.

Examiner

David B. Lugo

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 24 January 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 2,4,5,8,11,14,16-18,21,23-25,29,31,32 and 34-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 2,4,5,8,11,14,16-18,21,23-25,29,31,32 and 42 is/are allowed.
- 6) ☒ Claim(s) 34-38,40 and 41 is/are rejected.
- 7) ☒ Claim(s) 39 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments filed 1/24/05 have been fully considered but they are not persuasive.
2. Regarding claims 34 and 40, Applicant argues that the cited prior art fails to teach "a tone ordering element configured to assign bits to at least a portion of the tones in an interleaved manner such that adjacent tones have different bit densities" or "assigning data bits to at least a portion of the tones in an interleaved manner such that adjacent tones have different bit densities." Specifically, Applicant states that although Tzannes discloses a BAT where the bit density on one tone is different from the bit density for an adjacent tone, and Helms et al. disclose a tone interleaver, Helms et al. does not disclose that the bits are assigned such that adjacent tones have different bit densities. However, it is the combination of Tzannes with Helms et al. that is considered to disclose all the limitations of the claims. As admitted by Applicant, Tzannes already discloses a BAT where bits assigned to adjacent tones have different bit densities. When the tone interleaving of Helms et al. is used in the system of Tzannes, the bits assigned to the tones will maintain the property of having adjacent tones with different bit densities. Applicant is arguing that Helms et al. by itself does not disclose the recited limitation, but one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).
3. Regarding claim 37, Applicant argues that the cited prior art fails to teach "a tone ordering element comprising...logic for interleaving at least a portion of those bits assigned to

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adjacent tones.” Applicant asserts that the interleaver in Helms et al. cannot interleave bits assigned to adjacent tones since the interleaving occurs before the bits are assigned to tones. However, the claim does not require that the bits are first assigned to tones prior to interleaving, but only requires that the bits have been interleaved, where the bits are assigned to adjacent tones. Helms et al. includes an interleaver 325 provided in the transmit path for interleaving bits supplied thereto. Tone ordering circuitry 330 generates and orders the discrete multi tones of the modem. Since the bits assigned to the multi tones have been interleaved, the tone ordering circuitry 330 includes tones where the bits assigned to adjacent tones have been interleaved. Helms et al. is thus considered to disclose a tone ordering element as recited in claim 37.

4. Regarding claim 35, Applicant believes that it is allowable since it is dependent from claim 34. However, since the rejection of claim 34 is maintained, the rejection of claim 35 is also maintained.

5. Regarding claim 41, it is noted that Applicant has not presented any arguments regarding its rejection. However, in as much as any of Applicant’s arguments made with respect to claim 37 may apply to claim 41, reference is made to the response to those arguments.

6. The rejection of claims 34-38, 40 and 41 is maintained and restated below.

***Claim Rejections - 35 USC § 103***

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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8. Claims 34, 36-38, 40 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tzannes U.S. Patent 6,498,808 in view of Helms et al. U.S. Patent 6,144,695 (submitted by applicant).

9. Regarding claim 34, Tzannes discloses a transmitter in Figure 3 including a bit allocation table (BAT), shown in Table 1 (col. 2, lines 16-38), illustrating that each of a series of tones is associated with a bit density, and the number of bits assigned to each tone is different from the number of bits assigned to the adjacent tones, thereby resulting in different bit densities, wherein the BAT also contains the gain for each subchannel (col. 20, lines 1-10).

10. Tzannes does not expressly disclose a tone ordering element configured to assign bits to at least a portion of the tones in an interleaved manner.

11. Helms et al. disclose a tone ordering element 330 in the dual latency DMT system of Fig. 3A, considered to be configured to assign bits to at least a portion of the tones in an interleaved manner.

12. It would have been obvious to one of ordinary skill in the art to use a tone ordering element as disclosed by Helms et al. in the dual latency system of Tzannes, in order to comply with the ANSI standard (Helms et al., col. 2, lines 40-42) as Helms et al. further state that tone ordering circuitry is necessary for generating and ordering the discrete multi tones of a DMT modem (col. 3, lines 1-3).

13. Regarding claim 36, Tzannes discloses that the receiver sends a BAT to the transmitter (Fig. 4 – block 440), which may be adapted during system operation (block 420, col. 12, lines 43-44, col. 13, lines 29-44).

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14. Regarding claim 37, Tzannes discloses a transmitter in Figure 3 including a bit allocation table (BAT), as shown in Table 1 (col. 2, lines 16-38), illustrating that each of a series of tones is associated with a number of bits, wherein the BAT also contains the gain for each subchannel (col. 20, lines 1-10).

15. Tzannes does not expressly disclose a tone ordering element comprising logic for assigning each of the bits to one of the tones according to the bit and gain information, and logic for interleaving a portion of the bits assigned to adjacent tones.

16. Helms et al. disclose a tone ordering element 330 and an interleaver 325 in the dual latency DMT system of Fig. 3A, and is considered to assign bits to tones, and interleave at least a portion of the assigned bits.

17. It would have been obvious to one of ordinary skill in the art to use a tone ordering element as disclosed by Helms et al. in the dual latency system of Tzannes, in order to comply with the ANSI standard (Helms et al., col. 2, lines 40-42) as Helms et al. further state that tone ordering circuitry is necessary for generating and ordering the discrete multi tones of the DMT modem (col. 3, lines 1-3).

18. Regarding claim 38, the bits assigned to each tone are determined according to the noise on the subchannels (col. 1, lines 61-65).

19. Regarding claim 40, Tzannes discloses a transmitter in Figure 3 including a bit allocation table (BAT), shown in Table 1 (col. 2, lines 16-38), illustrating that each of a series of tones is associated with a bit density, and the number of bits assigned to each tone is different from the number of bits assigned to the adjacent tones, thereby resulting in different bit densities, wherein

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the BAT also contains the gain for each subchannel (col. 20, lines 1-10). Tzannes further discloses that the BAT is received at the transmitter (Fig. 4 – block 440, col. 13, lines 29-44).

20. Tzannes does not expressly disclose assigning bits to at least a portion of the tones in an interleaved manner.

21. Helms et al. disclose a tone ordering element 330 in the dual latency DMT system of Fig. 3A, considered to be configured to assign bits to at least a portion of the tones in an interleaved manner.

22. It would have been obvious to one of ordinary skill in the art to use a tone ordering element as disclosed by Helms et al. in the dual latency system of Tzannes, in order to comply with the ANSI standard (Helms et al., col. 2, lines 40-42) as Helms et al. further state that tone ordering circuitry is necessary for generating and ordering the discrete multi tones of the DMT modem (col. 3, lines 1-3).

23. Regarding claim 41, Tzannes discloses a transmitter in Figure 3 including a bit allocation table (BAT), as shown in Table 1 (col. 2, lines 16-38), illustrating that each of a series of tones is associated with a bit density, wherein the BAT also contains the gain for each subchannel (col. 20, lines 1-10) and the bit and gain information is assigned to the tones. Tzannes further discloses that the BAT may be sent to the transmitter from a receiver (Fig. 4 – blocks 440, 450, col. 13, lines 29-44), and further disclose that the method may be embodied in a computer program contained in a computer readable medium (e.g. claim 49).

24. Tzannes does not expressly disclose assigning each of the bits to one of the tones according to the bit and gain information and interleaving a portion of the bits assigned to adjacent tones.

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25. Helms et al. disclose a tone ordering element 330 and an interleaver 325 in the dual latency DMT system of Fig. 3A, and is considered to assign bits to tones, and interleave at least a portion of the assigned bits.

26. It would have been obvious to one of ordinary skill in the art to use a tone ordering element as disclosed by Helms et al. in the dual latency system of Tzannes, in order to comply with the ANSI standard (Helms et al., col. 2, lines 40-42) as Helms et al. further state that tone ordering circuitry is necessary for generating and ordering the discrete multi tones of the DMT modem (col. 3, lines 1-3).

27. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tzannes in view of Helms et al. as applied to claim 34 above, and further in view of Levin U.S. Patent 5,822,374 (previously cited).

28. Regarding claim 35, Tzannes and Helms et al. disclose a DMT communication system as described above, but do not expressly disclose raising the power on a first group of tones and lowering the power on a second group of tones in the bit assignment.

29. Levin discloses a method for fine gains adjustment in an ADSL system in Fig. 7 where a gain of a bin is adjusted up while a gain of another bit is adjusted down by a corresponding amount.

30. It would have been obvious to one of ordinary skill in the art to use the fine gain adjustment of Levin in the DMT system of Tzannes and Helms et al. in order to provide the best BER without changing the transmit power (Levin, col. 2, lines 42-53).

***Allowable Subject Matter***

31. Claims 2, 4, 5, 8, 11, 14, 16-18, 21, 23-25, 29, 31, 32 and 42 are allowed.
32. Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

***Conclusion***

33. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David B. Lugo whose telephone number is 571-272-3043. The examiner can normally be reached on M-F; 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Lugo  
6/1/05

  
**KHAI TRAN**  
**PRIMARY EXAMINER** 6/2/05